REMARKS

Claims 1, 2, 4-8, 10-14 and 16-19 are pending in the present application. Claims 2, 7, 8, 13 and 14 have been amended. Claim 19 has been presented herewith. Claims 3, 9 and 15 have been canceled.

Claim Rejections-35 U.S.C. 112

Claims 2, 7-12 and 14 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite. This rejection is respectfully traversed for the following reasons.

Applicant asserts that the term "high" in claims 2, 8 and 14 should not be construed as rendering the claims indefinite, as suggested by the Examiner. As described beginning on page 6, line 4 of the present application with respect to Fig. 1(C), a known high-energy ion-implantation technique can be used to form a source region, whereby an N-type impurity 106 such as arsenic is implanted with an energy amount of 500 keV. Applicant respectfully submits that one of ordinary skill, in light of the specification and in view of common knowledge with the art, would readily understand the scope and meaning of a high-energy ion-implantation. However, claims 2, 8 and 14 have been amended to feature a high-energy ion-implantation "with an energy amount that is about 500 keV", merely for the purpose of expediting prosecution of this application. Applicant respectfully submits that claims 2, 7, 8, 10-12 and 14 are in compliance with 35 U.S.C. 112, second paragraph, and thus respectfully urges the

Examiner to withdraw this rejection.

Drawings

The drawings have been objected to as allegedly failing to comply with 37 C.F.R. 1.84(p)(4), because reference characters "104" and "104a" have both been used to designate first insulating film. This objection to the drawings is respectfully traversed for the following reasons.

Applicant respectfully emphasizes that Fig. 1(B) of the present application illustrates first insulating film 104 as having a thickness of about 5000 Å as described on page 5, lines 7-16 of the application, and first insulating film **104b** as having a thickness of about 200 Å. Since reference numerals 104 and 104b respectively designate portions of first insulating film having respectively different thicknesses, Applicant respectfully submits that the use of reference characters 104 and 104b should be clear and acceptable. Applicant respectfully submits that the drawings are in compliance with 37 C.F.R. 1.84(p)(4), and thus respectfully urges the Examiner to withdraw this objection.

Claim Rejections-35 U.S.C 102(b)

Claims 1, 2, 5-8, 11-14, 17 and 18 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Efland et al. reference (U.S. Patent No. 5,736,766). This rejection is respectfully traversed for the following reasons.

The method of manufacturing an LDMOS transistor of claim 1 includes in combination "implanting ions of the first conductivity type into a part of the well region" and "forming a gate oxide layer on the surface of the semiconductor substrate, said forming the gate oxide layer including subjecting the semiconductor substrate to a heat treatment so that the implanted ions are diffused to form a diffusion region of the first conductivity type on the surface of the semiconductor substrate". As further featured, said implanting ions "is carried out with an energy set so that an accelerated oxidation during said forming the gate oxide layer is inhibited". Applicant respectfully submits that the Efland et al. reference as relied upon by the Examiner does not disclose these features.

Applicant initially emphasizes that said forming a gate oxide layer of claim 1 necessarily occurs **subsequent** to said implanting ions, because the heat treatment performed during said forming the gate oxide layer diffuses the previously implanted ions to form a diffusion region.

On page 3 of the current Office Action dated October 1, 2003, the Examiner has alleged that the Efland et al. reference describes in column 3, lines 61-63 with respect to Fig. 4 "implanting ions of the first conductivity type into a part of the well region with an energy". However, contrary to the Examiner's assertion, the above noted portion of the Efland et al. reference as particularly relied upon by the Examiner does not describe implantation. That is, the above noted portion of the Efland et al. reference describes a drive-in step that is performed **to diffuse** n and p type implants of previously formed

Dwell 44 so that the deeper p-type implant forms the Dwell backgate/channel region 46 while the shallower n-type implants form n-type source regions 48.

Accordingly, column 3, lines 61-63 of the Efland et al. reference as relied upon by the Examiner does not describe implanting ions. This particular portion of the Efland et al. reference as relied upon by the Examiner describes a drive-in step that diffuses previously implanted ions. Applicant therefore respectfully submits that the method of manufacturing an LDMOS transistor of claim 1 distinguishes over the Efland et al. reference as relied upon by the Examiner, and that this rejection of claims 1, 2, 5 and 6 is improper for at least these reasons.

With further regard to this rejection, the Examiner has alleged that column 4, lines 25-28 as described with respect to Figs. 5 and 6 of the Efland et al. reference, disclose "thermally growing a gate oxide layer 56 on the surface of the semiconductor substrate, diffusing the implanted ions to form a diffusion region 46 of the first conductivity type on the surface of the semiconductor substrate".

However, since gate oxide layer 56 is formed over Nwell 38 several process steps after the above noted drive-in step performed to diffuse the n and p type implants in Dwell 44 to form Dwell backgate/channel region 46 and source regions 48, the subsequent formation of gate oxide layer 56 clearly does not diffuse implanted ions to form a diffusion region 46 as alleged by the Examiner. Particularly, the implanted ions are diffused prior to formation of gate oxide layer 56, so that diffusion does not occur during gate oxide formation, as would be necessary to meet the features of claim 1.

Accordingly, Applicant respectfully submits that the method of manufacturing an LDMOS transistor of claim 1 distinguishes over the Efland et al. reference as relied upon by the Examiner, and that this rejection of claims 1, 2, 5 and 6 is improper for at least these additional reasons.

The method of manufacturing an LDMOS transistor of claim 7 includes in combination "implanting ions of the second conductivity type into a part of the second well region", and "forming a gate oxide layer on the surface of the semiconductor substrate, said forming the gate oxide layer including subjecting the semiconductor substrate to a heat treatment so that the implanted ions are diffused to form a diffusion region of the second conductivity type on the surface of the semiconductor substrate within the second well region". Independent claim 13 includes somewhat similar features. As noted above, since gate oxide layer 56 in Fig. 6 of the Efland et al. reference is formed well after the drive-in step that is performed to diffuse the implants, the Efland et al. reference as relied upon by the Examiner clearly does not disclose the above noted features of respective claims 7-13. Applicant therefore respectfully submits that the respective methods of manufacturing an LDMOS transistor of independent claims 7 and 13 distinguish over the prior art as relied upon by the Examiner, and that this rejection of claims 7, 8, 11-14, 17 and 18 is improper for at least these reasons.

Claim Rejections-35 U.S.C. 103(a)

Claims 3, 4, 9, 10, 15 and 16 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Efland et al. reference. Applicant respectfully submits that the Efland et al. reference as herein considered by the Examiner does not overcome the above noted deficiencies as set forth above. Applicant therefore respectfully submits that claims 4, 10 and 16 would not have been obvious in view of the prior art as relied upon by the Examiner for at least these reasons, in addition to the reasons as set forth previously.

Claim 19

The method of manufacturing an LDMOS transistor of claim 19 includes in combination "implanting ions of the second conductivity type into a part of the second well region", and "forming a gate oxide layer on a surface of the semiconductor substrate, said forming the gate oxide layer including subjecting the semiconductor substrate to a heat treatment so that the implanted ions are diffused to from a diffusion region of the first conductivity type on the surface of the semiconductor substrate as a source region". Applicant respectfully submits that claim 19 distinguishes over and would not have been obvious in view of the prior art as relied upon by the Examiner for at least somewhat similar reasons as set forth above with respect to claim 1.

Conclusion

Applicant respectfully submits that since the claims distinguish over the relied upon prior art for at least the above reasons, the corresponding amendments have been made merely to improve claim form, rather than to further distinguish over the relied upon prior art. Accordingly, the above noted amendments should not be construed as narrowing scope within the meaning of *Festo*.

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of one (1) month to February 1, 2004, for the period in which to file a response to the outstanding Office Action. The required fee of $110.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

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